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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,101	10/14/2003	Tsuyoshi Takahashi	30391-501	4465

7590

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EXAMINER

BATAILLE, PIERRE MICHE

ART UNIT

PAPER NUMBER

2186

DATE MAILED: 02/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/685,101

Applicant(s)

TAKAHASHI, TSUYOSHI

Examiner

Pierre-Michel Bataille

Art Unit

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/349,320.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Specification

1. This Office Action is responsive to Applicant's communication filed January 24, 2005 responding to ton Final-Action dated September 22, 2004. Applicant's amendment and/or arguments have been considered with the results that follow.
2. Claims 1-12 are present in the application under prosecution.
3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors.

The clause "each belonging to a group (e.g. claim 1, 2...) appears to lack antecedent basis in the claims. It is not clear which one of 'the plurality of blocks" or "the physical addresses" belong to the group.

Please note that these are merely exemplary. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Response to Arguments

4. Applicant's arguments with respect to claims 1-12 have been fully considered but are moot in view of the new ground(s) of rejection.

Independent claims 1, 2, 9-10, 11, 12 have been amended to remove the Nguyen's reference (US 6,568,526) from reading upon the claims, therefore

necessitates a new ground of rejection, which is made Final necessitated by the amendment.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,230,233 (Lofgren et al).

With respect to claims 1, 2, and 9-12, Nguyen teaches data processing system comprising a flash memory whose storage area has a plurality of blocks assigned physical addresses and each belonging to a group ***[(memory system of a general computer system including flash EEPROM memory array 11 whose operation is controlled by a memory controller 13) Fig. 1; Col. 3, Lines 5-8]***, and an access apparatus which performs acquisition of data from the flash memory, erasure of data from the flash memory and storage of data into the flash memory ***[the memory controller 13 managing operations (Write and erase operations) of the EEPROM memory 11) Col. 3, lines 10-15]***, wherein:

data stored in said blocks of said flash memory can be erased only in block units at once ***[Col. 6, Lines 49-53 (a block being the smallest group of***

cells that is erasable or programmable at one time) Col. 2, Lines 20-21; (all erase gates of the cells in each block are connected together for block erase) Col. 3, Lines 23-24];

said access apparatus comprises a memory and a controller **[flash EEPROM memory array 11 whose operation is controlled by a memory controller 13, Fig. 1; Col. 3, Lines 5-8];**

said memory stores an address translation table which shows the physical addresses assigned to the blocks belonging to one of said groups and logical addresses associated with said physical addresses **[(an address translation table 27 indicating logical address associated to physical memory address) Fig. 2; Col. 3, Lines 33-42],** and

said controller performs:

(1) acquiring logical addresses specifying the blocks which store the data to be acquired or the blocks which store the data to be erased **[Blocks of data received from the computer system with indication of user's logical address of a memory location, 23, Fig. 2; Col. 3, Lines 31-35],**

(2) determining whether it is possible to specify the physical addresses associated with the logical addresses acquired by said controller, and specifying among said groups a group of storage areas assigned the physical addresses associated with the acquired logical addresses **[the logical address is converted by an address translation table 27 into a physical memory address indicating the block within the memory 11 into which the data is to**

be written) Col. 3, Lines 35-42]; and accessing the blocks assigned the specified physical addresses [address translation table 27 converting the given logical address into a corresponding physical address of a block within the memory 11 that is to receive that data) Col. 3, Lines 35-42];

(3) updating the address translation table so as to show the physical addresses assigned to the specified group of blocks and the logical addresses associated with said physical addresses ***[(the address translation table is updated to result in directing data blocks directed to memory bank) Col. 3, Lines 23-26];***

(4) specifying the physical addresses associated with the logical addresses acquired by said controller, based on the updated address translation table and the acquired logical addresses, and accessing the blocks assigned the specified physical addresses ***[(Logical addresses causing its associated data block to be written into block having a physical address within a bank will cause the block to be written within the bank) Col 5, Lines 26-31].***

With respect to claims 3, Nguyen teaches said flash memory stores condition-defined data specifying conditions for access to the flash memory and said controller acquires the condition-defined data from the flash memory, and performs acquisition of data from the flash memory and erasure and storage of data other than the condition-

defined data from and into the flash memory in accordance with the conditions specified by the condition-defined data as acquired **[Col. 4, Lines 1-37; Col. 5, Lines 1-0]**.

With respect to claims 4-5, Nguyen teaches storage of replacement data representing contents of a replacement for a to-be-replaced portion of the condition-defined data, and said controller accesses the flash memory in accordance with the conditions specified by the condition-defined data, acquired from the flash memory and whose to-be-replaced portion has been replaced with the replacement data **[Col. 6, Lines 30-62; Col. 5, Lines 19-31]**.

With respect to claims 6-7, Nguyen teaches the access apparatus with the flash memory including identification data stored therein for identifying the flash memory and said controller acquires the identification data from the flash memory and determines whether to access the flash memory in accordance with the identification data as acquired **[Col. 5, Lines 19-31; Col. 6, Lines 30-62]**.

With respect to claim 8, Nguyen teaches said controller creating an empty area table specifying the blocks which do not store said data, among said plurality of blocks, storing the empty area table in said memory and causing the blocks specified by the empty area table to store said data **[Col. 5, Lines 21-40]**.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4281. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

February 9, 2005

PIERRE BATAILLE
PRIMARY EXAMINER